Lead-free Green

36V / 3A Synchronous Buck Converter

Description

JBR1433 is a synchronous buck converter with wide input voltage range (4 ~ 36V) and output current up to 3A. While the output voltage can be varied between 0.8V and 32V, the duty cycle can go up to 96% to support heavy load if necessary. Response to voltage transient at the output is quick due to the current-mode control loop and its ability to synchronize to an external clock as high as 2MHz.

To ensure reliable and safe operation, soft-start at 2ms typically, input under-voltage lock-out, and output current limiting on cycle-by-cycle basis are built in. Upon the detection of short-circuit, the device shall enter hiccup mode. Once the hazard condition expires, normal operation is resumed. Additional safeguard is provided by thermal shut-down as soon as the junction temperature approach 150°C. Featuring the PG (power good) and EN / Sync function, applicability of the device are greatly enhanced. JBR1433 is manufactured [halogen, lead, antimony] free and RoHS compliant. Packages offered: DFN3030-8L.

Features and Benefits

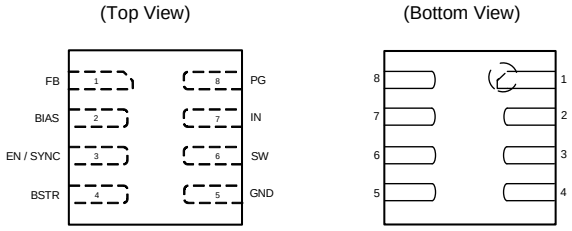
- Wide range of input voltages at 4 ~ 36V
- Continuous output current at up to 3A
- Fast transient response with built-in current-mode control loop
- Internal clock at 410kHz nominally and ability to synchronize to an external clock at frequency up to 2.4MHz
- Duty cycle at 96% maximum with minimum ON-time at 90ns
- Power-saving mode to reduce standby consumption to 5μA
- Comprehensive protection features built-in: input under-voltage lock-out, output current limiting, short-circuit, thermal shut-down
- Application-friendly features: soft-start, power-good, device-enable
- Lead-free package assembled with 'green' molding compound

Applications

- Voltage down-conversion in system where line voltage is ≤ 30V
- Gate driving in battery-powered hand tools & vacuum cleaners, AC-powered multi-function printer/scanner, etc.
- Non-isolated power source on mainboard in industrial controls, factory equipment, network equipment, etc.

Pin Assignment

DFN3030-8L



Ordering Information

JBR1433 X

Product Prefix | Package

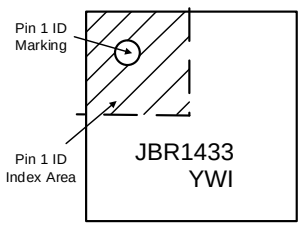
DC: DFN3030-8L

Product Name	Package	Marking	MSL	T_J (°C)	Media	Quantity (pcs)
JBR1433DC	DFN3030-8L	JBR1433	3	-40 ~ 125	13" T&R	5,000

Marking Information

(Top View)

DFN3030-8L



First Line: Marking (see *Ordering Information*)

Second Line: Date Code
Y: Year of Molding
W: Work-week of Molding
I: Internal Code

Pin Description

Pin #	Pin Name	Type	Function
1	FB	I	Feedback. It is connected to center tap of resistor divider at VOUT. Once V_{FB} drops below 660mV, F_{SW} is lowered to prevent runaway of current limit in case of short-circuit condition.
2	BIAS	O	Bias Supply. Capacitor of 0.1 ~ 0.22μF is populated here for de-coupling purpose.
3	EN / SYNC	I	Enable/Ext. Sync. Pulled 'H' to enable operation. F_{SW} is aligned to the external clock appeared here
4	BSTR	I	Bootstrap. Floating supply voltage for driver to internal high-side MOSFET. Capacitor of 0.1μF is recommended between SW and BSTR to minimize the switching spikes.
5	GND	-	Device Ground. This is the ground reference for the device. It should be carefully connected to the ground plane with copper trace(s) and via(s) wherever appropriate.
6	SW	O	Switching Terminal: Thick copper trace should be used accordingly.
7	IN	-	Supply Voltage. This should be connected with thick copper trace to the input voltage source. A decoupling capacitor connected to GND shall stabilize the input voltage level.
8	PG	O	Power Good. Active-high open-drain output. 'H' indicates that the output voltage exceeds 90% of its nominal value. When unused, it should be tied to GND.

Typical Application Circuit

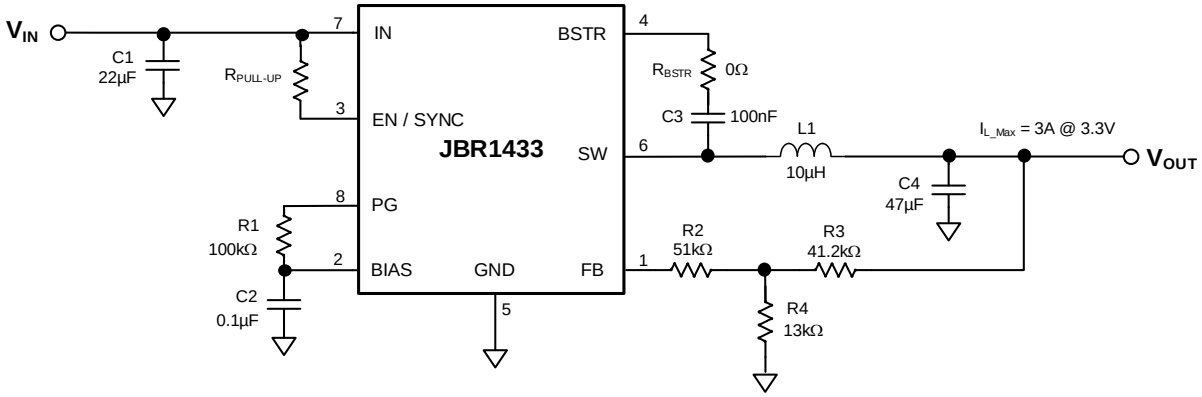


Fig. 1: Application Circuit

Functional Blocks

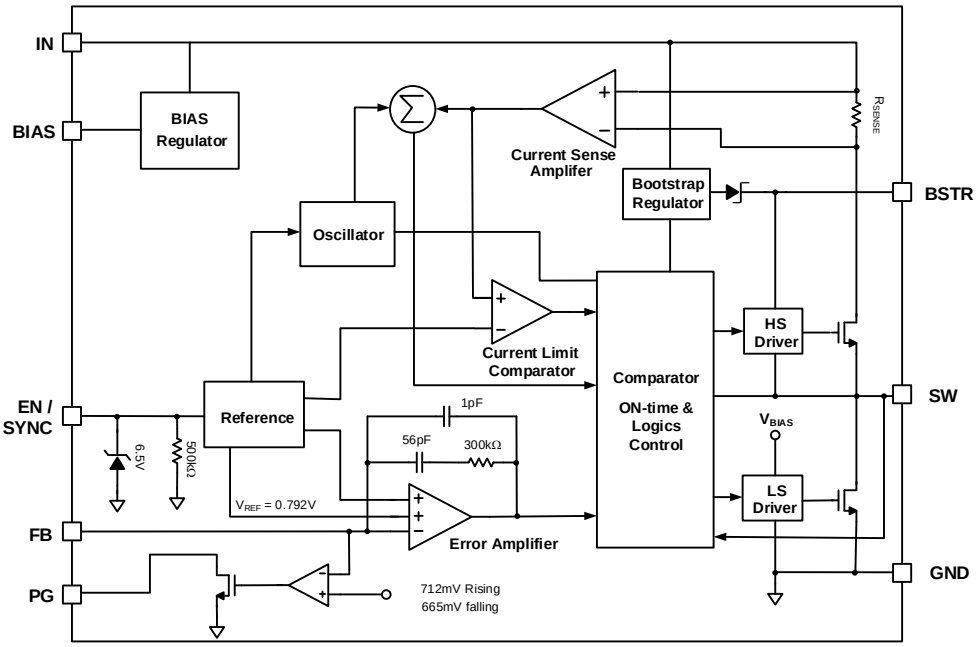


Fig. 2: Diagram of Internal Functional Blocks

Absolute Maximum Ratings (All measurements were made at T_A = 25°C unless otherwise stated)

Symbol	Parameter	Conditions	Values	Unit
V_{IN}	Input Voltage Range	-	-0.3 ~ 40	V
V_{SW}	Switching Output Voltage Range	-	-0.3 ~ 41	V
V_{BSTR}	Bootstrap Output Voltage Range	-	V_{SW} + 6	V
T_J	Operating Junction Temperature	-	172	ºC
T_{STG}	Storage Temperature Range	-	-40 ~ 150	ºC
P_D	Continuous Power Dissipation @ T_A = 25°C	DFN3030-8L	2.27	W
HBM	ESD (Human Body Model)	-	± 2.5	kV

Recommended Operating Conditions (All measurements were made at T_A = 25°C unless otherwise stated)

Symbol	Parameter	Values	Unit
V_{IN}	Continuous Supply Voltage	4 ~ 36	V
V_{OUT}	Output Voltage	0.8 ~ 0.9 x V_{IN}	V
T_J	Operating Junction Temperature Range	-40 ~ 125	ºC

Electrical Characteristics

Test Conditions [V_{IN} = 12V; T_A = 25°C] are applicable to the following measurement unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SHDN}	Supply Current (shut-down)	V_{EN} = 0V	-	-	5	μA
I_Q	Supply Current (quiescent)	V_{EN} = 2V; V_{FB} = 1V	-	0.4	0.6	mA
$R_{DS(ON)-H}$	High-side Switch ON-Resistance	$V_{BSTR-SW}$ = 5V	-	76	96	mΩ
$R_{DS(ON)-L}$	Low-side Switch ON-Resistance	V_{CC} = 5V	-	50	70	mΩ
I_{LKG-SW}	Leakage Current at High/Low-side Switch	V_{EN} = 0V; V_{SW} =12V	-		1	μA
I_{LIMIT}	Current Limit	Duty Cycle < 40%	3.2	4.5	5.5	A
f_{SW}	Oscillator Frequency	V_{FB} = 750mV	320	410	500	kHz
f_{FB}	Fold-Back for Switching Frequency	V_{FB} < 400mV	70	100	130	kHz
DC_{Max}	Maximum Duty Cycle	V_{FB} = 750mV; f_{SW} = 410kHz	92	96	-	%
t_{ON-Min}	Minimum ON-time of High-side Switch		-	90	-	ns
f_{SYNC}	Frequency Range of External Clock		0.2	-	2.4	MHz
V_{FB}	Feedback Voltage		778	792	806	mV
$V_{EN-Rise}$	Threshold of EN, Rising		1.15	1.39	1.65	V
$V_{EN-Fall}$	Threshold of EN, Falling		1.05	1.26	1.45	V
V_{EN-Hys}	Hysteresis of EN Threshold		-	130	-	mV
I_{EN}	Input Current for Device Enable	V_{EN} = 2V	-	4.0	6.0	μA
		V_{EN} = 0V	-	0.0	0.2	μA
$UVLO_{Rise}$	UVLO Threshold-Rising		3.3	3.5	3.7	V
$UVLO_{Fall}$	UVLO Threshold-Falling		3.1	3.3	3.5	V
$UVLO_{Hys}$	UVLO Threshold-Hysteresis		-	200	-	mV
V_{BIAS}	BIAS Voltage	I_{CC} = 0mA	4.6	5.0	5.2	V
$BIAS_{LR}$	Load Regulation	I_{CC} = 5mA	-	1.5	4.0	%
t_{SS}	Soft-Start Period	V_{OUT} rises from 10% to 90%	1	2	3	ms
T_{TSD}	Thermal Shutdown		150	-	-	°C
$T_{TSD-Hys}$	Thermal Hysteresis		-	30	-	°C
$PG_{TH-Rise}$	PG Threshold-Rising	percentage of V_{FB}	86	90	94	%
$PG_{TH-Fall}$	PG Threshold-Falling	percentage of V_{FB}	80	84	88	%
PG_{TH-Hys}	PG Threshold-Hysteresis	percentage of V_{FB}	-	6	-	%
$t_{PGDLY-Rise}$	Rising Delay of PG		60	130	200	μs
$t_{PGDLY-Fall}$	Falling Delay of PG		30	55	95	μs
V_{PG}	Sink Current Capability of PG pin	Sink Current = 4mA	-	0.1	0.3	V
I_{LKG-PG}	Leakage Current at PG pin		-	10	100	nA

Note 1: Performance are guaranteed by design hence the parameter was not subject to FT during manufacturing.

Thermal Properties

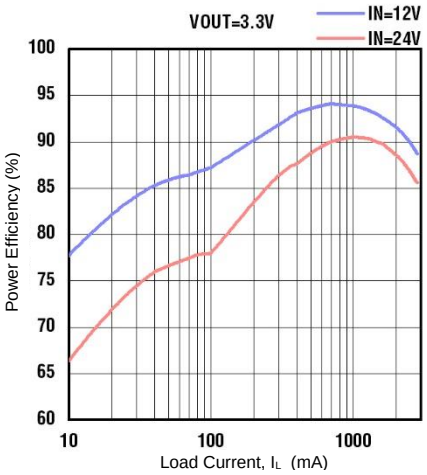
Test Conditions: Device mounted on FR-4 substrate, 2-layer PCB, 2oz copper, with minimum recommended cooling pad to dissipate heat

Symbol	Parameter	Package	Rating	Unit
$R_{\Theta JA}$	Thermal Resistance (junction-to-ambient)	DFN3030-8L	55	°C/W

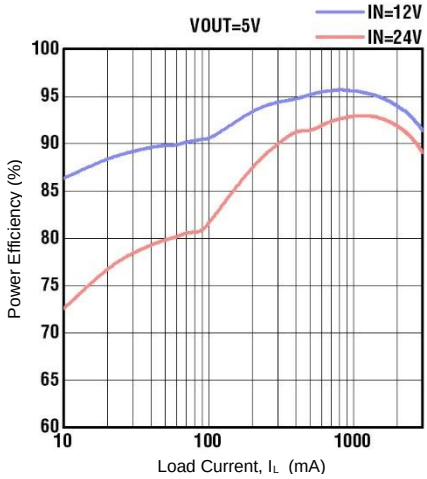
Typical Performance Characteristics

Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; L1 = 10µH; T_A = 25°C

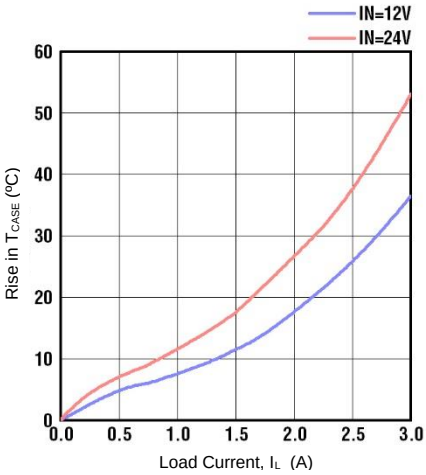
Graph 1: Power Efficiency at V_{OUT} = 3.3V



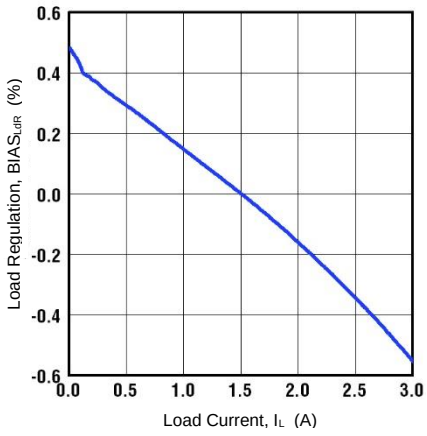
Graph 2: Power Efficiency at V_{OUT} = 5.0V



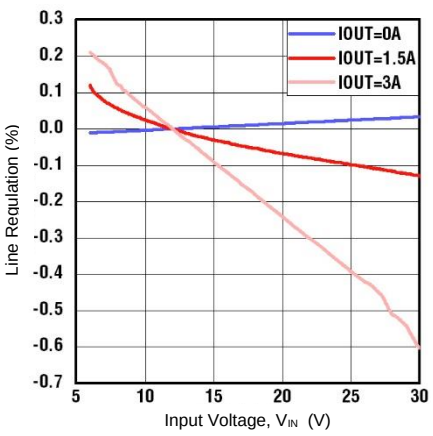
Graph 3: T_A vs. Load Current



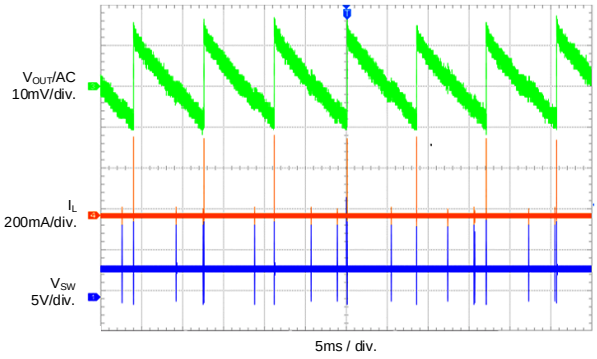
Graph 4: Load Regulation at V_{OUT} = 3.3V



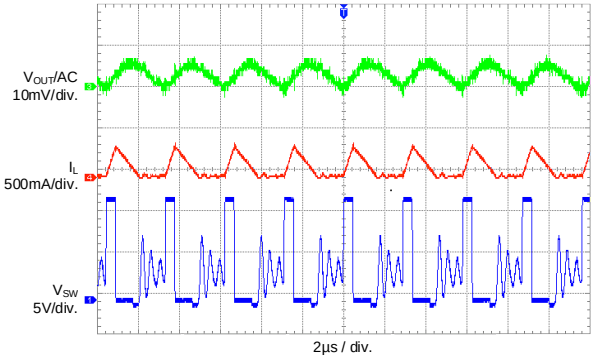
Graph 5: Line Regulation at V_{OUT} = 3.3V



Graph 6: Steady State with I_{OUT} = 0A



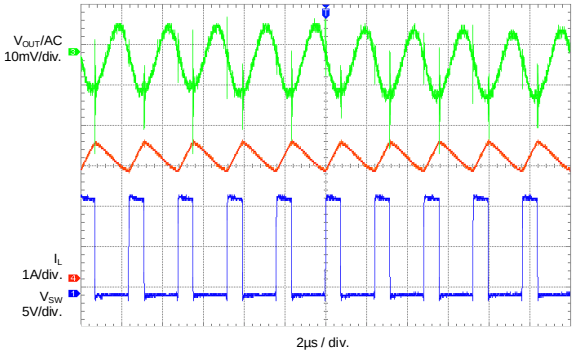
Graph 7: Steady State with I_{OUT} = 0.1A



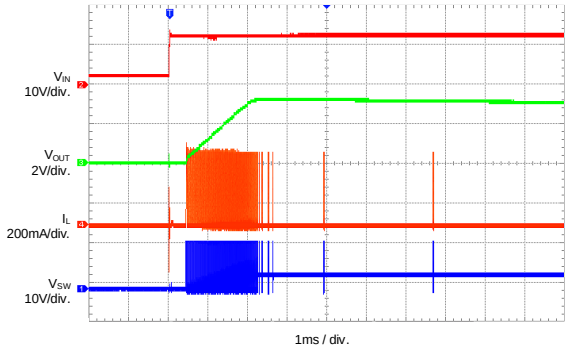
Typical Performance Characteristics (Continued)

Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; L1 = 10µH; T_A = 25°C

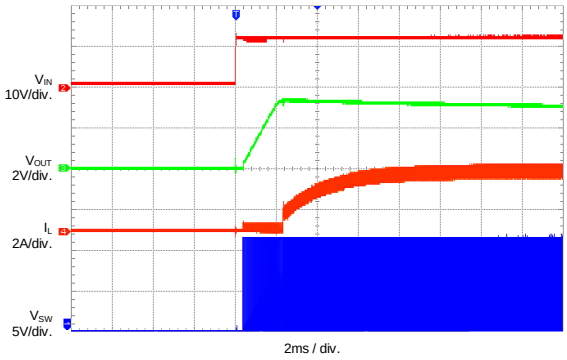
Graph 8: Steady State with I_{OUT} = 3A



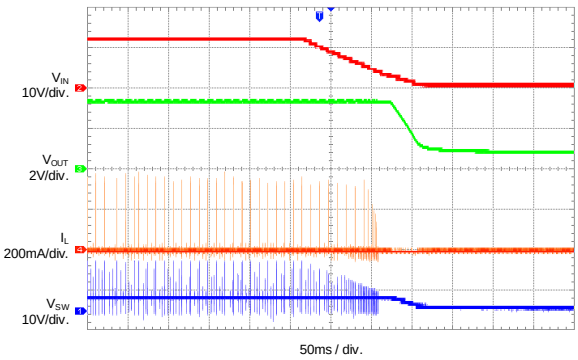
Graph 9: Start-up at IN with I_{OUT} = 0A



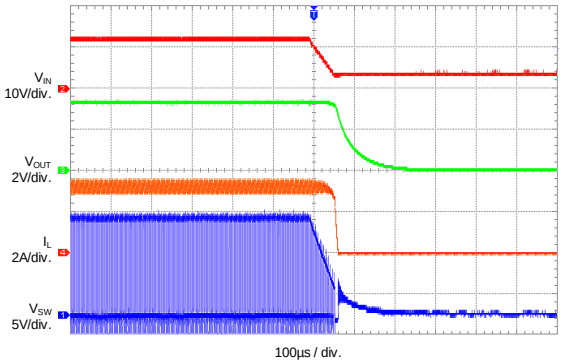
Graph 10: Start-up at IN with I_{OUT} = 3A



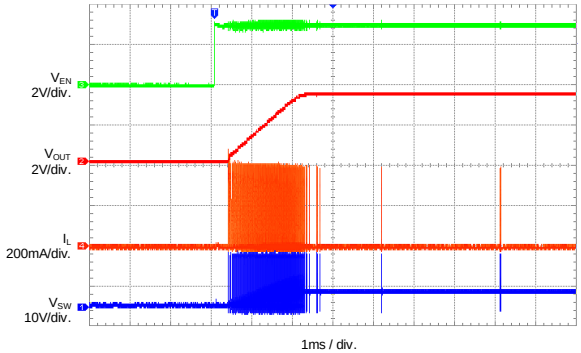
Graph 11: Shut-down at IN with I_{OUT} = 0A



Graph 12: Shut-down at IN with I_{OUT} = 3A



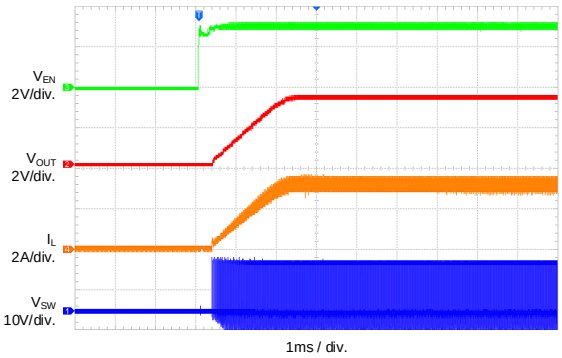
Graph 13: Start-up at EN with I_{OUT} = 0A



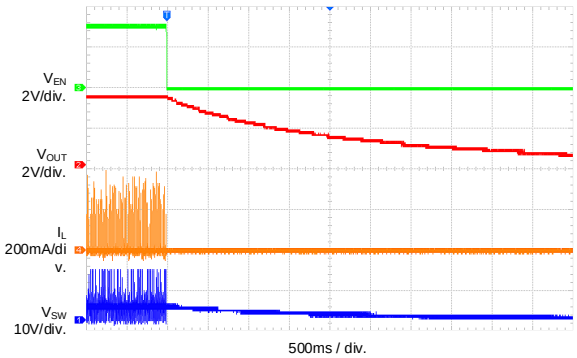
Typical Performance Characteristics (Continued)

Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; L1 = 10µH; T_A = 25°C

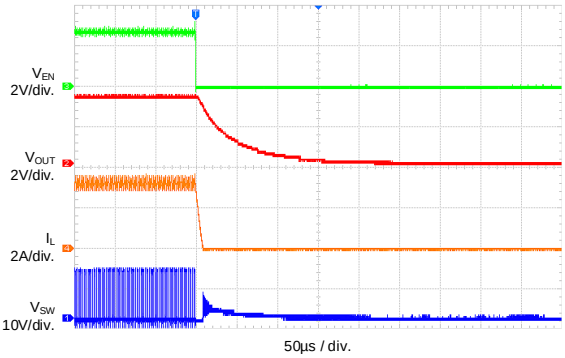
Graph 14: Start-up at EN with I_{OUT} = 3A



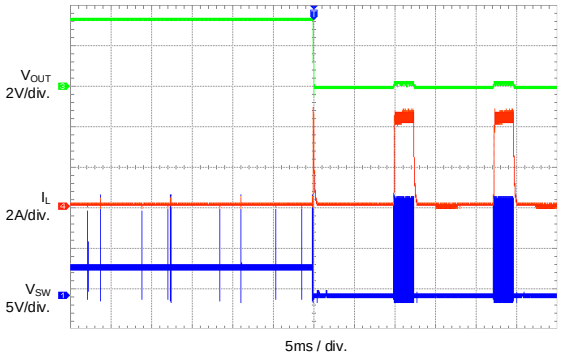
Graph 15: Shut-down at EN with I_{OUT} = 0A



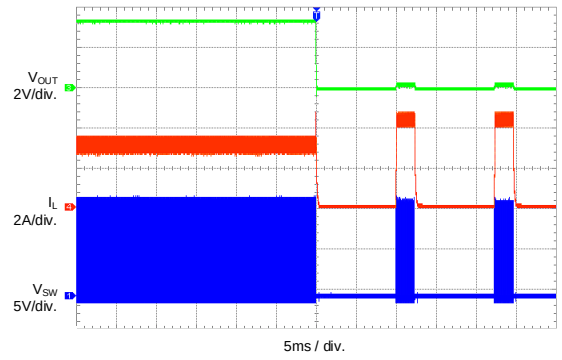
Graph 16: Shut-down at EN with I_{OUT} = 3A



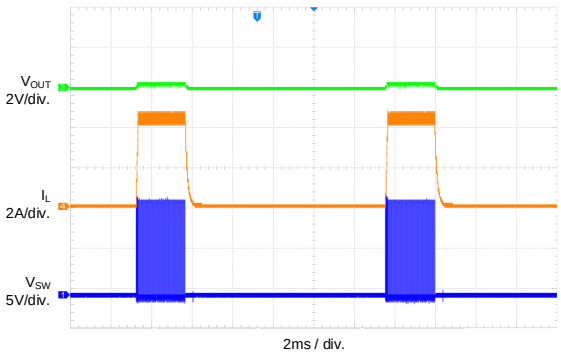
Graph 17: Short-circuit Protection (from 'I_{OUT} = 0A' to 'SC Entry')



Graph 18: Short-circuit Protection (from 'I_{OUT} = 3A' to 'SC Entry')



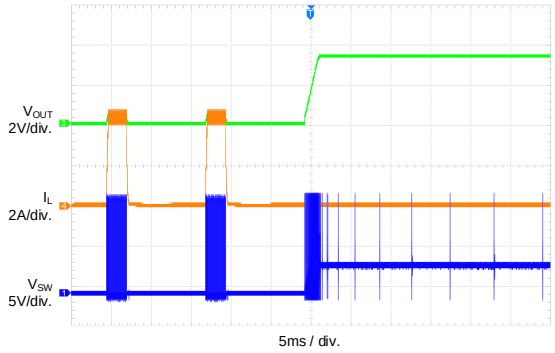
Graph 19: Short-circuit Protection Recurring



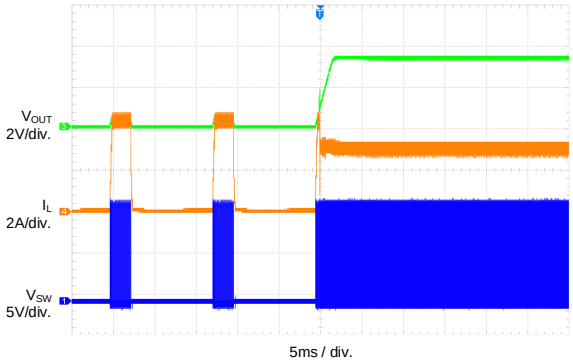
Typical Performance Characteristics (Continued)

Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; L1 = 10µH; T_A = 25°C

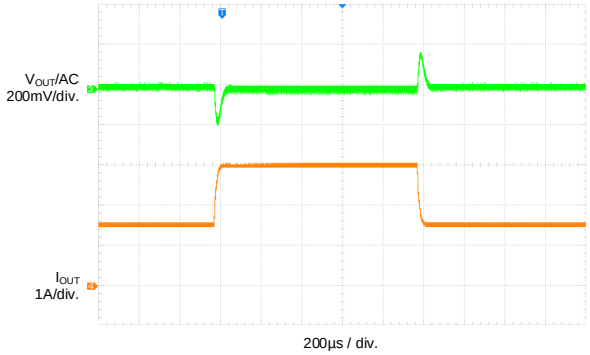
Graph 20: Recovery fr. Short-circuit Protection (SCP to 'I_{OUT} = 0A')



Graph 21: Recovery fr. Short-circuit Protection (SCP to 'I_{OUT} = 3A')



Graph 22: Load Transient @ 1.6A/µs (I_{OUT} varied btw. 1.5A & 3A)



Detailed Description of Device Operation

Overview

JBR1433 is a synchronous step-down (buck) converter in which the high-side and low-side power switches are embedded. Innovative assembly technology is employed to offer 3A continuous output current from a highly compact low-profile surface-mounted type package of 3mm x 3mm.

The device switches at the rising edge of each PWM cycle which is dictated by an internally generated clock (nominal frequency at 410kHz). Optionally, the device can synchronize (at the rising edges) to an external clock (maximum frequency at 2.2MHz recommended) appearing at the EN / SYNC pin. The internal current-mode control loop regulates the output voltage and responds swiftly to any changes at the load. At each PWM cycle, the high-side switch (i.e. power MOSFET) turns ON until the current reaches the value set by the internal Current Limit Comparator. Under the circumstances in which the value is not reached within D_{MAX} within the same PWM cycle, the switch shall be turned OFF.

BIAS Regulator

This unit is powered by the supply voltage appeared at the IN pin. It supplies regulated power (nominal voltage at 5V) to all the circuit blocks inside the device. Full regulation are achieved as long as V_{IN} stays above 5V. If ever V_{IN} falls below 5V, output of this unit shall follow suit accordingly. MLCC of 0.1μF is recommended to populate between BIAS pin and GND pin for de-coupling purpose.

Error Amplifier

Voltage appeared at FB pin, i.e. V_{FB}, is compared to V_{REF} which is generated internally and of nominal value 0.792V. Output of the Error Amplifier controls the current going out of the SW pin.

EN / SYNC Control

EN / SYNC is a digital input which is used to turn ON / OFF the device. A logic 'H' at the pin shall turn the device ON, while a logic 'L' at the pin shall turn the device OFF.

Inside the device, a resistor of 500kΩ and zener diode of V_Z = 6.5V are populated between this pin and GND to ensure proper operation. The resistor practically forces the device to remain OFF even if this pin is 'floated', i.e. unconnected. Pairing with a pull-up resistor connected between IN pin and this pin shall limit the input current at the pin to less than 150μA. If this pin is tied directly to the IN pin without the presence of $R_{PULL-UP}$, V_{IN} must not exceed 6V to prevent possible damage to the zener diode behind. As an illustration, assuming V_{IN} = 12V, the value of the resistor can be calculated as shown below:

$R_{PULL-UP} \geq (12V - 6.5V) \div 150\mu A = 36.7k\Omega$

Whenever an external clock (200kHz ~ 2.4MHz) is fed into this pin, the pulse width must be > 200ns to ensure proper operation.

Under-voltage Lock-out (UVLO)

The UVLO Fault Detection unit shall pull all the output pins to 0V whenever the input voltage, V_{IN}, falls below a preset threshold. This unit monitors the output voltage of the internal BIAS Regulator. The UVLO Exception flag is asserted when V_{BIAS} falls to 3.3V and below. The flag is dis-asserted once V_{BIAS} rises to 3.5V and beyond.

Soft-start (SS)

This SS unit prevents the output of the device from over-shooting when the device is started up. Every time the device starts up, V_{SS} is generated. It shall ramp up from 0V to 1.2V. Before the value of V_{SS} reaches the value of V_{REF} (nominally at 0.792V), V_{REF} is replaced by V_{SS} at the input of the Error Amplifier unit. Once [$V_{SS} > V_{REF}$] becomes true, the Error Amplifier unit reverts to normal operation and uses V_{REF} as the reference input henceforth. Ramp-up time of V_{SS} is nominally 1.5ms by design.

Over-current Protection (OCP) and Hiccup-Mode (HM) of Operation

This unit monitors the output current at SW pin continuously. When the output current over the inductor connected to SW pin goes up beyond the current limit threshold, V_{OUT} starts to fall. Once the value V_{FB} becomes less than the threshold set by UVLO (typically at ~ 84% of V_{REF}), hiccup-

Detailed Description of Device Operation (Continued)

mode shall be triggered with the output current subsequently dropped to zero. Thereafter, the device shall resume typical operation at the rising edge of the next PWM cycle. If the current limit threshold continues to be exceeded, HM shall be re-triggered again. On the other hand, the device shall exit HM if the output current stays below the current limit threshold. In the situation of persistent dead-short in the application circuit, this arrangement significantly reduces the average short-circuit current and thermal build-up in the proximity of the device.

Thermal Shut-down (TSD)

When the device is operating in its typical manner, the temperature (i.e. T_J) of the silicon die assembled inside the package inevitably heats up. This unit shall shut down the device to prevent damage from overheat once T_J is found to exceed 170°C. When the value of T_J drops below a lower threshold (e.g. ~ 140°C), the device shall resume normal operation.

Start-up (SU) and Shut-down (SD)

When the voltage appearing at the IN and EN pins match the designated values (refer to Electrical Characteristics section of this data sheet), the device starts up (SU). The BIAS Regulator unit shall start first because it supplies stable voltage and current to the rest of the units inside the device. The Reference unit follows suit and generates the reference voltage on which many key logic decision depend upon.

The device is forced to shut down (SD) whenever one of the following conditions become TRUE:

1. Logic '0' appearing at the input of EN / SYNC pin
2. Voltage level at the IN pin is below the UVLO threshold
3. Value of Tj is higher than the T_{TSD} threshold value

Once the SD procedure is in progress, all the fault detection units shall be disabled. All the internal regulators are turned OFF gracefully in an orderly manner to ensure the completion of SD.

Power Good (PG)

Though the monitoring of V_{REF}, this open drain output (drain terminal of an internal MOSFET) indicates if the output voltage is in good order. This pin should be tied to the BIAS pin through a resistor of about 100kΩ.

At power-up, before the SS (soft-start) unit is in full swing, output of the PG pin shall remain at logic '0' Once the value of V_{FB} reaches 90% of V_{REF}, output of PG will be pulled to logic 'H' at a delay of 90μs later. Whenever the value of V_{FB} drops to the level at 84% of V_{REF}, output of the PG pin shall be pulled to logic '0' again.

The output of the PG pin shall be pulled to logic '0' when either TSD is asserted or the input signal at the PIN / SYNC pin is at logic '0'.

Power-saving Scheme (PSC) at Light Load

When light load appears at the output of the application circuit, the device shall carry out the buck conversion under the discontinuous conduction mode (DCM). During DCM operation, the low-side switch shall be turned OFF whenever the output current approaches zero. Such arrangement further reduces the current consumed by the device.

Application Information

Setting Output Voltage

Generally, output voltage (V_{OUT}) of the device is set by a resistor divider (R3 and R4 in Fig. 1) whose center tap is connected to the FB pin. The resistor, R3, also determines the bandwidth of the feedback loop in conjunction with the compensation capacitance behind the FB pin. Assuming R3 of 41.2kΩ, the value of R4 shall be calculated using the formula shown below:

$R4 = R3 / [(V_{OUT} / 0.792) -1]$

Indeed, the T-type Resistor Network shown in Fig. 1 is deemed more appropriate for low value of V_{OUT}. Similar to the typical case, the sum of R1 and R2 determine the bandwidth of the feedback loop. The larger the aggregated value, the lower the bandwidth. To ensure loop stability, the bandwidth should be limited to 40kHz assuming the default switching frequency of 410kHz. The table below illustrates the recommended values for R1, R2, and R3:

V_{OUT} (V)	R1 (kΩ; ± 1%)	R2 (kΩ; ± 1%)	R3 (kΩ; ± 1%)
3.3	51.00	41.20	13.00
5.0	51.00	41.20	7.68

Selection of Inductor

For most applications, the inductor connected to the SW pin shall fall between 1 ~ 10μH, and carry DC current rating of at least 25% higher than the maximum load current. The smaller the DC resistance of the inductor, the higher the efficiency. As a guidance, the formula shown below can be used to estimate the inductance best fit for the application environment:

$L_1 = [V_{OUT} \times (V_{IN} - V_{OUT})] / (V_{IN} \times \Delta I_L \times f_{SW})$; where ΔI_L is the inductor ripple current

By default, the inductor ripple current shall be approximately 30% of the I_{L_Max}. Under the condition of light load (I_L < 100mA), power efficiency can be improved with larger inductor value. The formula shown below can be used to calculate the I_{L_Max}:

$I_{L\_Max} = I_L + (\Delta I_L / 2)$

Setting UVLO Threshold for V_{IN}

When the voltage at the IN pin falls below 3.3V, all the internal units with the exception of the UVLO unit shall be turned OFF. Once the voltage at the IN pin rises above 3.5V, all the internal units shall resume normal operation. For applications in which higher UVLO thresholds are required, an external resistor divider network can be connected to the IN and EN / SYNC pins as shown in Fig. 3 below:

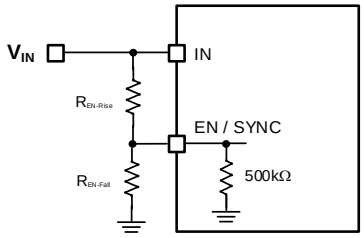


Fig. 3: Resistor Divider for Fine-tuning UVLO Thresholds

The UVLO thresholds can be calculated using the equations shown below. In order to ensure that the current sunk into the EN / SYNC pin is less than 150mA, the value of REN-UP must be sufficiently large.

$UVLO_{Rise} = V_{EN\text{-}Rise} \times [1 + R_{EN\text{-}Rise} / (500k\Omega \,//\, R_{EN\text{-}Fall})]$; where $V_{EN\text{-}Rise} = 1.39V$

$UVLO_{Fall} = V_{EN\text{-}Fall} \times [1 + R_{ENRise} / (500k\Omega \,//\, R_{EN\text{-}Fall})]$; where $V_{EN\text{-}Fall} = 1.26V$

Application Information (Continued)

Selection of Input Capacitor

Because the current supplied into the device for the DC-DC down conversion is dis-continuous, a capacitor is required at the IN pin to maintain a stable DC input voltage supply. It must have enough capacitance to provide sufficient charge such that excessive voltage at the IN pin can be avoided. The input voltage ripple resulted from presence of the input capacitor can be estimated by the formula shown below:

$$\Delta V_{IN} = [I_L / (f_{SW} \times C1)] \times (V_{OUT} / V_{IN}) \times [1 - (V_{OUT} / V_{IN})]$$

Either one of the following three types of building materials can be considered for the input capacitor: electrolytic, tantalum, ceramic. For best effect, MLCC with X6S or X7R dielectrics is recommended due to their inherent properties of low ESR and smaller temperature coefficient. In most applications, capacitance of 22μF suffices the need for stable DC voltage supply. In order to by-pass the high frequency switching noise, especially when electrolytic or tantalum type of input capacitor is selected, a minuscule (e.g. package size 0603) high-quality MLCC with low value (e.g. 1μF) is recommended closely between the IN and the GND pins. The p.c.b. section in the later part of this document provides a good reference for the layout consideration.

Because the input capacitor C1 (c.r.: Fig. 1) inevitably absorbs the input switching current, its ripple current rating must be adequate. The RMS current to be encountered by C1 can be estimated by the formula shown below:

$$I_{C1} = I_L \times \sqrt{(V_{OUT} / V_{IN}) \times [1 - (V_{OUT} / V_{IN})]}$$

The worse-case scenario probably happens at $V_{IN} = 2x\ V_{OUT}$ where $I_{C1} = I_{LOAD} / 2$. In general, an input capacitor with RMD current rating higher than half of the maximum load current is recommended.

Selection of Output Capacitor

The output capacitor, C4, is used to maintain stable output voltage at DC-level. Either one of the following three types of building materials can be considered for the output capacitor: electrolytic, tantalum, ceramic. In general, capacitor with low ESR shall be used in order for the output voltage ripple to be minimized. The output voltage ripple resulted from presence of the output capacitor can be estimated by the formula shown below:

$$\Delta V_{OUT} = [V_{OUT} / (f_{SW} \times L1)] \times [1 - (V_{OUT} / V_{IN})] \times \{R_{ESR\text{-}C4} + [1 / (8 \times f_{SW} \times C4)]\};$$

where L1 is the inductor value and $R_{ESR\text{-}C4}$ is the equivalent series resistance (ESR) of the output capacitor C4

When MLCC is used as the output capacitor, the capacitance shall dominate the impedance and contributes mostly to the output voltage ripple. The output voltage ripple resulted from presence of the MLCC output capacitor can be estimated by the formula shown below:

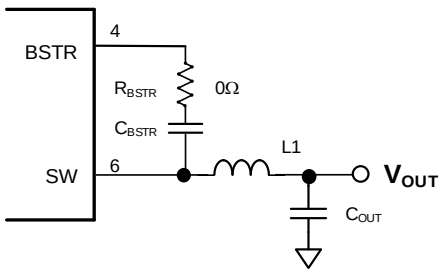
$$\Delta V_{OUT} = [1 - (V_{OUT} / V_{IN})] \times [V_{OUT} / (8 \times f_{SW}^2 \times L1 \times C4)]$$

When either tantalum or electrolytic capacitor is used as the output capacitor, the ESR shall dominate the impedance and contributes mostly to the output voltage ripple. The output voltage ripple resulted from presence of either tantalum or electrolytic output capacitor can be estimated by the formula shown below:

$$\Delta V_{OUT} = [V_{OUT} / (f_{SW} \times L1)] \times [1 - (V_{OUT} / V_{IN})] \times R_{ESR\text{-}C4}$$

Bootstrap Resistor

An optional bootstrap resistor, R_{RSTR}, populated between the BSTR pin and C_{RSTR} can effectively reduce the spike voltage present at the SW pin. Nonetheless, care must be taken with the resistance applied. In general, while the reduction of spike voltage is better with higher resistance, the lower the power efficiency turns out to be.



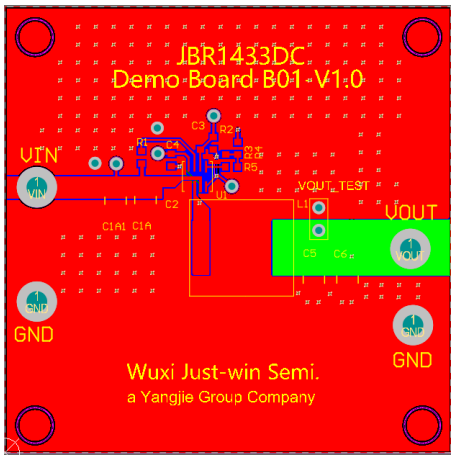
Application Information (Continued)

Layout of Bill of Materials (BOM) in Applications

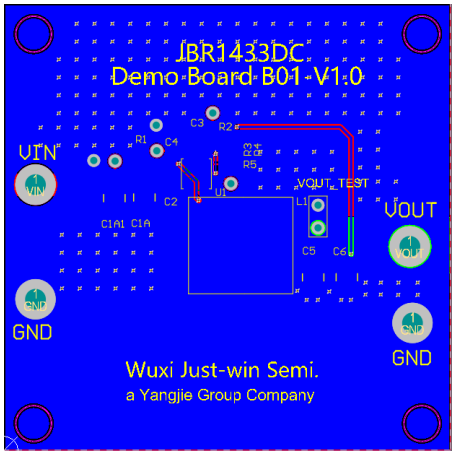
For p.c.b. layout, placement of the capacitors at the IN and BIAS pins are important. To achieve the best effect, the guidelines shown below should be followed:

1. Input capacitor, C1, should be placed as close as possible to the IN and GND pins. Likewise, the minuscule (e.g. 0603 body size) MLCC used to by-pass the high-frequency switching noise should also be placed closed to the IN and GND pins. Simultaneously, connection of these capacitors to the IN pin should be as short and as wide as possible.
2. The capacitor, C2, should be placed as close as possible to the BIAS and GND pins. The copper traces between VCC pin and C2, between C2 and the GND pin should also be made as short as possible.
3. GND pin shall be connected to a large ground plane directly. In case that the large ground plane is located at the bottom layer of the p.c.b., through-hole vias populated around the GND pin allow a virtually direct connection to the large ground plane.
4. The pcb traces to the SW and BSTR pins should be placed as far away as possible from pins (e.g. FB) which are sensitive to switching noises.
5. The T-type resistor divider is best placed close to the FB pin

Top Layer of JBR1433DC Demo Board



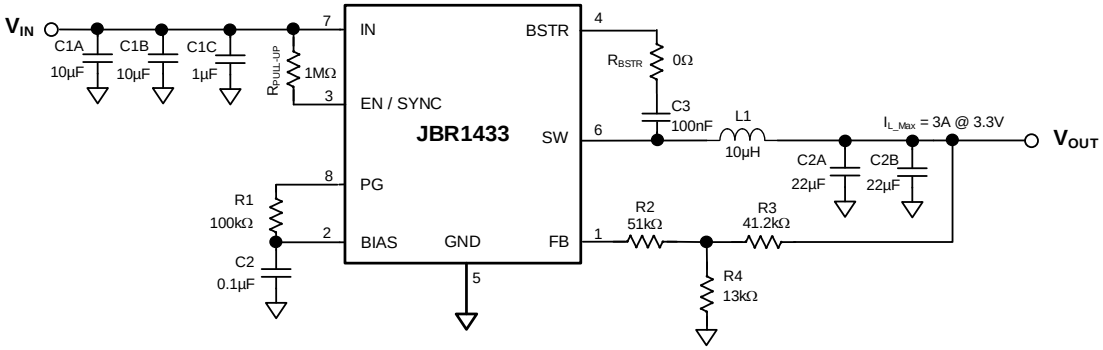
Bottom Layer of JBR1433DC Demo Board



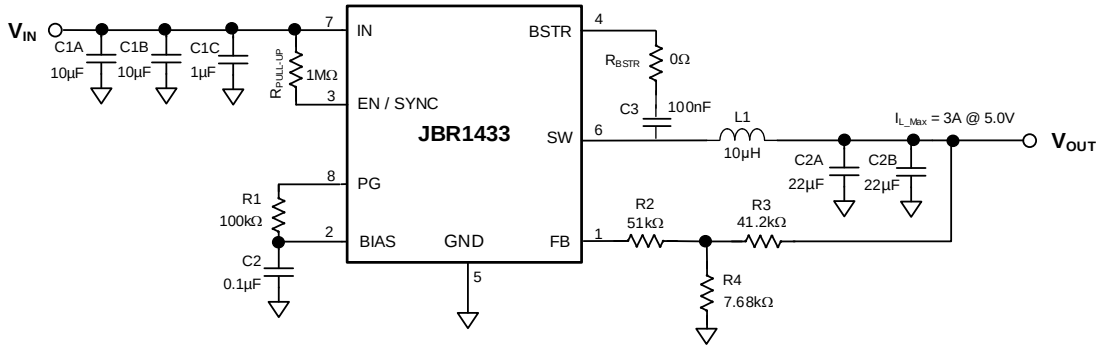
Application Information (Continued)

Typical Application Circuits

1. Condition: V_{IN} = 12V; V_{OUT} = 3.3V; I_L = 3A



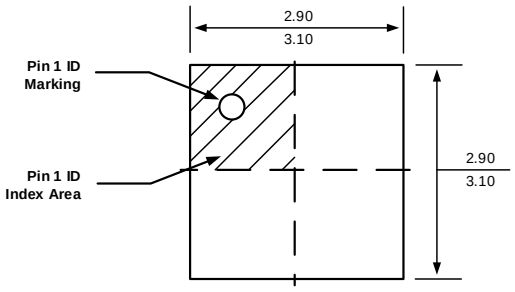
2. Condition: V_{IN} = 12V; V_{OUT} = 5.0V; I_L = 3A



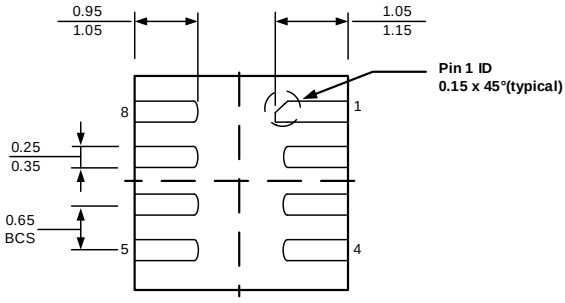
Package Outline (All measurements in mm)

Package Type: DFN3030-8L (J1)

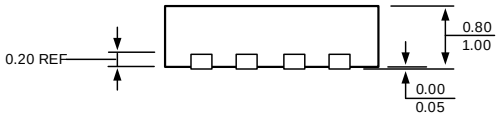
Top View



Bottom View

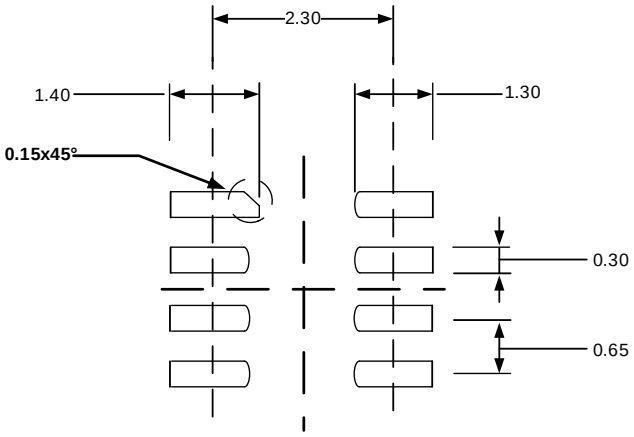


Side View



Suggested Pad Layout (All measurements in mm)

Package Type: DFN3030-8L (J1)



cc

Disclaimer

The information presented in this document are for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. (a.k.a. YJ) reserves the right to make changes without prior notice to the specification of the product displayed herein to improve reliability, function, design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices. It is not designed, intended, or authorized for use as a critical component in equipment or devices (e.g. medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices) which require high level of reliability and the malfunction of which directly endangers human life. YJ or anyone on its behalf assumes no responsibility or liability for any damages resulting from such improper use of the product.

This publication supersedes & replaces all information previously supplied. For additional information, please visit our website http://www.21yangjie.com, or consult your nearest YJ Sales Offices for further assistance.